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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR		ATTORNEY DOCKET NO.
08/650,628	05/20/96	EICHELBERGER	C	1109.001

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EXAMINER	
POTTER,R	

ART UNIT	PAPER NUMBER
2508	#5

DATE MAILED: 01/12/98

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary

Application No.	Applicant(s)
08/650,628	Eichelberger
Examiner	**Group Art Unit**
Roy Potter	2508

☒ Responsive to communication(s) filed on *Sep 3, 1997*.

☐ This action is **FINAL**.

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire *three* month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

Disposition of Claims

☒ Claim(s) *1-59* is/are pending in the application.

Of the above, claim(s) *25-55* is/are withdrawn from consideration.

☐ Claim(s) _____ is/are allowed.

☒ Claim(s) *1, 5, 6, 8-11, 13, 14, 17-22, 56, and 57* is/are rejected.

☒ Claim(s) *2-4, 7, 12, 15, 16, 23, 24, 58, and 59* is/are objected to.

☐ Claims _____ are subject to restriction or election requirement.

Application Papers

☒ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

☐ The proposed drawing correction, filed on _____ is ☐approved ☐disapproved.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☐ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number) _____.

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____.

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

☒ Notice of References Cited, PTO-892

☒ Information Disclosure Statement(s), PTO-1449, Paper No(s). *2*

☐ Interview Summary, PTO-413

☒ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

--- SEE OFFICE ACTION ON THE FOLLOWING PAGES ---

DETAILED ACTION

Applicant's election without traverse of claims 1 - 24 and 56 - 59 in Paper No. 4 is acknowledged.

Claim Rejections - 35 USC § 112

Claim 6 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 6, lines 4 - 6 recite "said release layer being thermally or chemically removable without removing said in situ processed layer". This is indefinite as the characteristics of the release layer cannot be determined.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 5, 13, 14, 17, 19, 20, 22 and 56-57 are rejected under 35 U.S.C. 102(b) as being anticipated by Fillion.

Fillion et al. discloses an electronic system package. As shown in Figure 2, the package comprises a plurality of chips 22. Each chip comprises an unpackaged chip having at least one

side surface, an upper surface, a lower surface and at least one contact pad 24 at the upper surface. A structural material, substrate 16, surrounds the side surface of each chip and mechanically interconnects in spaced planar relationship the plurality of chips 22. Substrate 16, as shown in Figure 2, has an upper surface 18 that is substantially co-planar with an upper surface of each chip of the plurality of chips to form a first substantially co-planar surface comprising a front surface. The lower surface of structural material 16 is substantially parallel with the lower surface of each chip 22 of the plurality of chips and forms a second surface comprising a back surface. A multi-layer high density interconnect (HDI) overcoat structure 26 is built up to interconnect the chips. The HDI overcoat structure 26 is built up to interconnect the chips. The HDI overcoat comprises a polyimide dielectric film 28 laminated across the top surfaces of the chips 22 and surface 18. Via holes 30 are located in film 28 in alignment with the contact pads 24 of chips 22. The first film 28 corresponds to the recited "in situ processed layer."

Claim 1, line 20 recites "an in situ processed layer". This is "product by process" claim language. The applicant should note that such claim language cannot be relied upon to patentably distinguish the present invention from the prior art. The same layer is recited in other parts of the claims, and has been interpreted as having a structural limitation only.

Claim 5 recites a multilayer structure over the in situ processed layer. The multilayer structure electrically interconnects at least some of the chips. Fillion et al. disclose a metallization layer 32 that extends over the film 28 and into via holes 30. Additional dielectric 28' and metallization layers 32' provide all the metallizations to the chips 22, interconnecting them.

Claim 13 recites that at least one chip in the multichip module comprises a bare chip. Claim 14 recites that each chip comprises a bare integrated circuit chip. The chips in the Fillion et al. device are bare chips.

Claim 17 recites that the in situ processed layer comprises a photo-patternable dielectric layer. The ability of polyimide to be photo-patterned is well known in the art and is an inherent characteristic of polyimide. Laser light is used by Fillion et al. to form vias in layer 28.

Claim 20 recites that the in situ processed layer comprises a photo-patternable dielectric material. The ability of polyimide to be photo-patterned is well known in the art and is an inherent characteristic of polyimide. Laser light is used by Fillion et al. to form vias in layer 28.

Claim 22 recites that the metallization structure comprises at least one I/O contact electrically coupled to a contact pad of the chip and being disposed at least partially over the structural material surrounding the chip. Fillion et al. discloses an I/O pad 40.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 8, 9, 10, 11, 18, 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fillion et al..

Claim 8 recites that the multilayer structure comprises a first multilayer structure and is disposed over the in situ processed layer on the front surface and a second multilayer structure is disposed on the back surface. Claim 9 is dependent on claim 8 and recites that the second multilayer structure comprises a preprocessed printed circuit board conductively secured to the back surface. Claim 10 is also dependent on claim 8 and recites that the multichip module comprises at least one conductive through connect disposed within the structural material and extending between the front surface and the back surface for interconnecting the first and second multilayer structures. Claim 11 recites at least one surface mount electronic component disposed on an exposed surface of at least one of the multilayer structures.

Fillion et al. teach a representative electrical contact pad 50 on the lower surface of structural material 16. To connect this lower contact pad to a multilayer structure such as a printed circuit board, which is well known in the art, would require only routine skill in the art. It would further be obvious to surface mount other components to the printed circuit board, as this is the conventional use of such boards.

Claim 18 recites that the structural material comprises a polymer consisting of one of epoxy, urethane, and polyimide. This is not taught by Fillion et al. Fillion et al. teach the use of a ceramic structural material, however, it is well known in the art to make substrates form other materials including epoxies, urethanes and polyimides.

Claim 21 recites that the structural material comprises a polymer consisting of one of epoxy, urethane, polyimide. Fillion et al. disclose that substrate 16 is ceramic. However, it is

well known in the art to make substrates form other materials including epoxies, urethanes and polyimides.

Allowable Subject Matter

Claims 2, 3, 4, 6, 7, 12, 15, 16, 23, 24, 58 and 59 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim 2 recites that the structural material has the same thickness as the thickest chip. This is not disclosed by Fillion et al. However, in column 4, lines 40 - 42 Fillion et al. state that "the individual cavities 20 are of appropriate depths for the various chips mounted therein." However, as the chips in the Fillion et al. package are attached at the bottom of the cavity, it would not have been obvious to make the structural material of Fillion et al. The same thickness as the thickest chip. The prior art does not teach or suggest the recited structure of claim 2.

Claim 3 recites that the multichip module further comprises an intrachip metallization layer comprising metal within each via electrically connected to a contact pad and the intrachip metallization fails to electrically interconnect any chips. Fillion et al. teach the interconnection of chips. The prior art does not teach or suggest the recited structure of claim 3.

Claim 4 recites that each chip has a common thickness and that the structural material has the same thickness. This would not have been obvious at least for the reasons given in regard to claim 2 above.

Claim 6 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112 set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

Claim 6 recites that the multilayer structure of claim 5 comprises a release layer. This is neither taught nor suggested by the prior art. Claim 7 is dependent on claim 6 and recites that the release layer comprises a thermoplastic transition layer disposed on the in situ processed layer. This is also not taught or suggested by the prior art.

Claim 12 recites that there is a surface mount component on each of the first and second multilayer and electrically coupled. The prior art does not teach or suggest such an arrangement.

Claim 15 recites that each chip of the module has an equal thickness with the upper surface of each chip coplanar with the front surface and the lower surface of each chip coplanar with the back surface. This is not taught or suggested by the prior art and would not have been obvious at least for the reasons given in regard to claim 2 above. Claim 16 is dependent on claim 15 and recites that the multichip module further comprises a heat sink in physical contact with the back surface. Fillion does not state that substrate 16 acts as a heat sink, however, as highly thermal conductive ceramic AlN is specified as a material of substrate 16, it would be inherent that it would act as a heat sink. However, claim 16 is dependent on a claim whose limitations are not taught or suggested by the prior art.

Claim 23 recites that the bottom surface of the structural material is substantially coplanar with the lower surface of the integrated circuit chip. This is not taught by Fillion et al. This would not have been obvious at least for the reasons given in regard to claim 2 above.

Claim 24 recites that back surface of the structural material comprises an exposed main surface of the integrated circuit module. This is not taught by Fillion et al. And would not have been obvious to one of ordinary skill in the art at the time the invention was made.

Claim 58 recites that the lower surface is substantially coplanar with the lower surface of the chips and claim 59 recites that a heat sink it attached to the lower surface. This is neither taught nor suggested by the prior art.

Conclusion

Papers related to this application may be submitted by facsimile transmission via the Art Unit 2508 Fax No. (703) 308 - 7723.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Roy Potter whose telephone number is (703) 308 - 4106.

Roy Potter
Patent Examiner
Group 2500

Potter
January 8, 1998